Development of SOI based MMICs for Wireless LAN Applications

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Abstract: Due to its improved RF performances over conventional CMOS technology, SOI technology is a promising candidate for front-end wireless transceiver circuits. This paper demonstrates the development of fully on-chip integrated SOI based MMICs for IEEE 802.11a standard. A modified BSIM model is developed to predict small signal RF behavior. The development of high Q on-chip inductor design and modeling is detailed. The low noise amplifier, implemented in a commercially available 0.35 μm SOI MOSFET process, is both input and output 50 Ohms matched and operates in C-band. It exhibits a forward gain (S21) of 10.5 dB with a noise figure of 4.5 dB while drawing 15 mA from a 1.8 V supply. The Doubly balanced Gilbert cell topology Mixer exhibits a peak gain of 7.5 dB and IIP3 of +11 dBm. It consumes about 11 mA from a 3.3V supply. To the best of our knowledge this research is the first report of SOI based implementation of MMICs for C-band wireless applications.

Index Term: RF SOI MOSFET, on-chip inductor, LNA, thermal noise, OFDM.

I. INTRODUCTION

In the recent years, there has been a lot of activities in developing IC solutions for wireless LAN applications in various unlicensed bands. Availability of 300MHz of bandwidth in 5-6 GHz frequency range has motivated researchers to investigate solutions for next generation wireless LAN applications [1]. This band uses Orthogonal Frequency Division Multiplexing (OFDM) modulation scheme. Due to immunity to intersymbol interference (ISI) and lower complexity in the baseband processing, it shows tremendous potential for applicability in next generation wireless LAN solutions. However, the multicarrier nature of OFDM signal results in high peak-to-average ratio which may drive the front end amplifiers into the saturation and make the system vulnerable to nonlinear distortion. Hence the receiver blocks must be designed to accommodate high input third-order intercept point (IIP3) with high dynamic range. It also requires low power consumption for long battery life.

SOI has emerged as an attractive technology for integrated RF circuit because of its better RF performances over conventional bulk-silicon technologies in terms of increased Ft and Fmax, decreased junction capacitance, improved sub-threshold slope, enhanced drive current, elimination of leakage path to substrate and adjacent devices. In addition the buried oxide allow implementation of higher Q-factor on chip passive components. These attributes overcome many of disadvantages associated with conventional bulk silicon CMOS technology for microwave applications. However, very little work has been reported on MMIC based on SOI technology to date [2-4]. In this paper, we present the first report of SOI based MMIC solutions for C-band wireless applications.

The fabrication process utilizes a 0.35 μm partially depleted SOI technology. The buried oxide thickness is 400nm. The gate oxide thickness is 8 nm and the silicon island thickness is 210 nm. The devices under study include floating body (FB) and body-tied type. Body tied devices have their body terminals tied to the source by means of implant that extend into the gate and is of the same type as the well. The well ties are shorted by simple abutment at the both ends of the gate.

II. Modified BSIM RF model development.

The BSIM3v3 model has become an industry standard for sub-micron MOSFETs. However it is still not capable of modeling the RF characteristics of sub-micron CMOS and SOI-CMOS transistors. Because impedance matching is crucial to RF circuits performances, the present BSIM3v3 model is inadequate for RF circuit design [5]. Therefore, to simulate the small-signal RF behavior, a modified BSIM3v3 model with a added substrate network has been proposed and validated with small signal S-parameters measurements from 1 to 10 GHz for both body tied and floating body devices. The substrate network is describe in figure 1, where Rg,Rs and

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Rd, Rbs are the gate, source, drain and body-to-source resistance respectively, Csub the body-to-substrate parasitic capacitance. As shown in figure 2, a good agreement with the measurements is achieved by this model. The gain is slightly underestimated, and input and output impedance are well predicted.

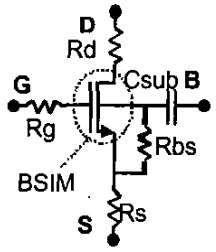

Fig. 1. Modified BSIM model.

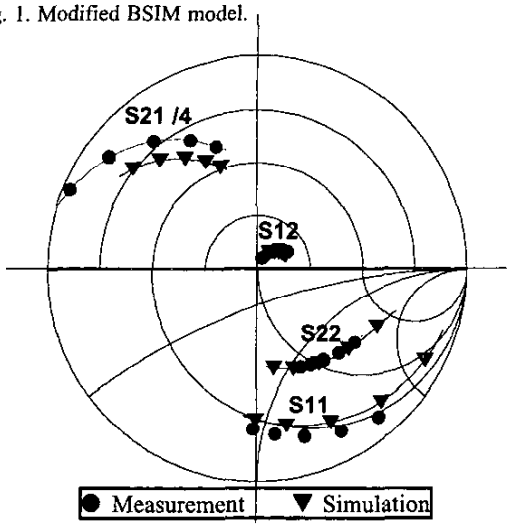

Fig. 2. Modified BSIM model S-parameters.

III. On-chip Passive Development

High Q-factor on-chip inductor plays an important role in microwaves circuit design for low power and low noise portable applications. Despite many efforts, Q-factor of on-chip inductors in conventional silicon substrates are typically low (<10) [6], essentially due to the substrate losses. In SOI technology, the buried oxide layer greatly reduces the parasitic capacitances to the substrate, increases the equivalent substrate resistance, and therefore leads to better inductor RF performances.

A die photograph of fabricated circular inductors we've developed is shown in Figure 3a. Figure 3b shows the equivalent circuit model commonly used for a circular inductor [7], where L denotes the series inductance and R accounts for the resistive loss. C models the capacitance between the metal lines. Csub1 and Csub2 are related to capacitive coupling between the coils and the substrate. Finally, Rsub1 and Rsub2 are the substrate resistances. According to the geometrical considerations and the model developed in [6-8] for the inductance value and the Q-factor calculation, a series of spiral inductors have been designed with different line widths, space, number of turns, and with one or two shunted metal layer. All metal layer are Al/Cu and exhibit sheet resistance lower than 0.05 Ω/ . In the case of the two shunted metal layer inductor, the top metal layer of a thickness of 1.5 μm is shunted with the bottom layer of a thickness of 0.6 μm thanks to array of small via (0.8 μm^2 each) spread along the coil. Thus, the parasitic resistances are reduced. The connection from the center of the coil to the output port has been implemented using the bottom metal layer. On-wafer calibration and measurements using vector-network analyzer have been performed. The inductance value and the Q-factor versus frequency are shown in Figure 4. The Q factor is obtained from Q= imag(Zin) / real(Zin), using the inductor input impedance Zin = 1 / Yin. A Q-factor up to 13 has been obtained, for an inductance value of 1.1 nH at the frequency of interest. The parameters of the inductors have been extracted. The results for a 1.5 and a 2.5 turn inductor are summarized in Table 1.

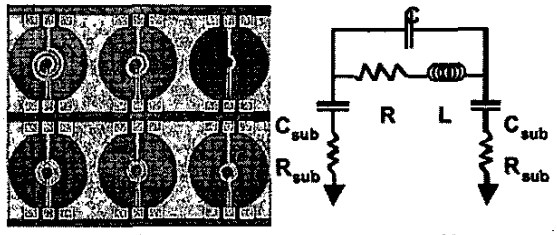

Fig. 3a. On-chip Inductors photo; 3b: Inductor model.

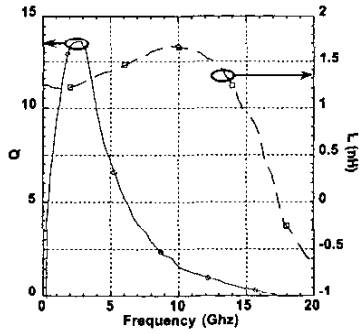

Fig. 4. 1.5 turn on-chip Inductor measurement results.

TABLE 1: On-chip inductors extracted parameters.

# of Spirals	L nH	R Ω	C fF	Cox pF	Rsub Ω	Fsr GHz
1.5	1.1	0.8	12	0.93	1130	> 40
2.5	2.1	1.4	21	1.85	960	~ 25

III. LNA Design

The linearity requirement of the LNA is driven by Adjacent Channel Interference (ACI), Alternate Adjacent Channel Interference (AACI) and the maximum power input at the receiver. According to the specifications [9], the IIP3 of the LNA must be optimized for a maximum input power level of -25 dBm. Also, the system requires a noise figure of 10dB. Hence, the LNA noise figure should be kept as small as possible. To avoid saturation of the mixer, the gain of the LNA should be kept above 10 dB.

The LNA is fully on-chip integrated and utilizes a single ended input single ended output 50 Ohms matched cascode topology with inductive degeneration. The inductive source degeneration technique, which has been demonstrated to exhibit minimum noise is attractive for achieving the input impedance matching (50 Ω), a critical requirement for the LNA. The cascode configuration is also advantageous in separating input and output matching criteria. Also it provides better stability in the LNA circuit.

For a given length of the device, channel width and the number of fingers are critical parameters because they determine the gate resistance Rg and therefore the LNA noise factor [10]. To optimize NF and gain, measurements have been done on 2, 6, 12, and 18 fingers 30 µm width SOI MOSFET devices. The minimum noise figure versus the bias conditions is shown in Figure 5. Hence, we've chosen to use a 12 fingers device at Vds = 1 to 2 V and Vgs = 1 V, leading to a power consumption less than 30 mW.

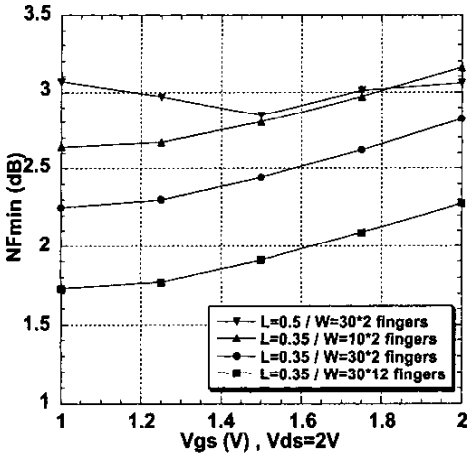

Fig. 5. Minimum Noise Figure for different devices.

The chip has been fabricated in Honeywell Semiconductor's 0.35 µm SOI MOSFET process and occupies about 1x1.3 mm^2. The measured performances exhibit a gain about 10.5 dB at 6.6 GHz and a 50 Ω noise figure about 4.5 dB. Input and output return losses are both greater than 15 dB at this frequency (Figure 6). Rollet stability factor condition, K>1, has been examined. Two tone IP3 analysis have been performed with 6.6 GHz and 6.61 GHz tones with equal power levels and exhibits an IIP3 of -5 dBm, figure 7. The LNA drawn about 15 mA from 1.8 V DC supply.

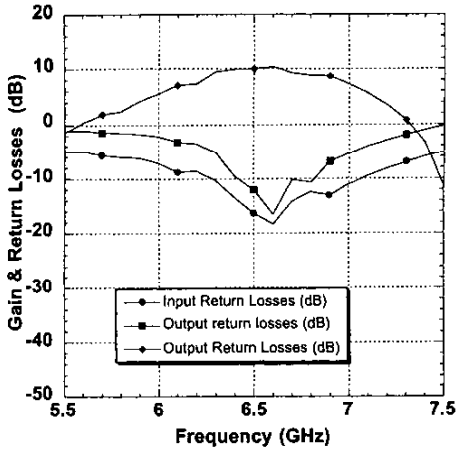

Fig. 6. Measured LNA's Gain and return losses.

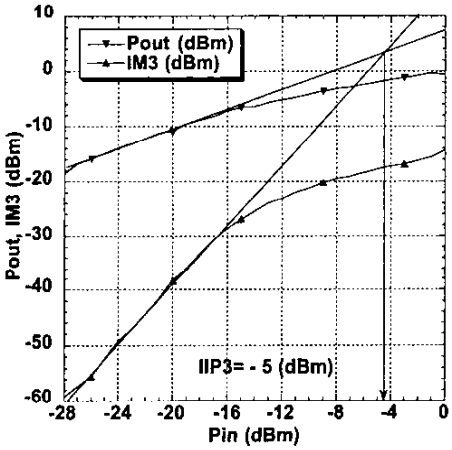

Fig. 7.Two tone IP3 of the LNA at f1=6.6 GHz and f2=6.61 GHz..

IV. Mixer design

Doubly balanced Gilbert cell topology has been chosen for the down conversion mixer. Biasing the mixer core FETs near threshold allows a reduced LO power for driving the FETs like ideal switches. Two such balanced mixers, with their LO signals in quadrature, can be used for down converted signals in quadrature. The device sizes of the mixer NFET transistors has been chosen to be 360 µm for achieving the desired gain from the mixer. Inductive degeneration has been used to achieve the

desired linearity performance. The input impedance of the MOS devices is dominated by gate to source capacitance for high frequency operation, hence the operating frequency of the mixer circuit must be lower than the series resonance circuit formed by degeneration inductor and gate to source capacitor of the MOS device as well as the self resonating frequency (SRF) of the degenerating inductor. The simulated mixer performance is shown in Fig 8. The LO and RF frequencies have been chosen as 5.7 and 5.8 GHz respectively, thus resulting in a very low IF signal of 100MHz at its output. It exhibits a peak gain of 7.5 dB and IIP3 of +11 dBm. It consumes about 11 mA from a 3.3V supply.

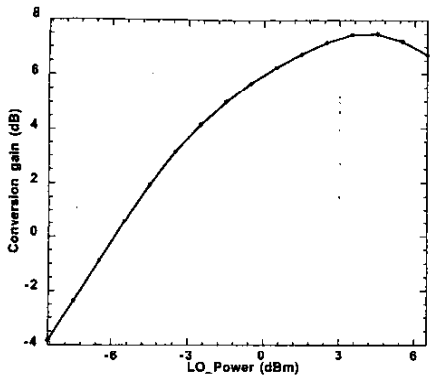

Fig. 8. Simulated Mixer conversion gain variation w.r.t. LO power

CONCLUSION

We have presented the first SOI based fully on-chip integrated front-end IC development for C-band wireless LAN applications. A modified BSIM model is developed to predict small signal RF behavior. Development of high Q-factor on-chip inductor has been presented. A fully on-chip integrated cascode LNA in 50-Ohms termination has been fabricated and doubly balanced Gilbert cell topology Mixer has been simulated. Measured performances indicate that the SOI based design can meet C-Band wireless applications specifications in term of gain, noise, linearity and consumption. To the best of our knowledge this is the first report of SOI based MMIC design efforts for C-band wireless standard.

Acknowledgements

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References

[1] S.Yoo, D. Heo, CH. Lee, B.Matinpour, S. Chakraborty, J.Laskar, "A 5.8 GHz OFDM GaAs MESFET MMIC chip set" *J.Microwave Symposium Digest. 2000 IEEE MTT-S International , Volume: 3 , 2000 Page(s): 1273 -1276 vol.3.*

[2]Song Ye, Salama, "A 1 V, 1.9 GHz, low distortion dual-gate CMOS on SOI mixer C.A.T". *SOI Conference, 2000 IEEE International , 2000 Page(s): 104 –105.*

[3]Harada, M. Tsukahara, T.Kodate, J. Yamagishi, A.Yamada, 5 "2-GHz RF front-end circuits in CMOS/SIMOX operating at an extremely low voltage of 0.5 V." *J. Solid-State Circuits, IEEE Journal of , Volume: 35 Issue: 12 , Dec. 2000 Page(s): 2000 –2004*

[4]Wei Jin, Weidong Liu, C. Hai, CH.Chan, Chenming Hu ,"Noise modeling and characterization for 1.5V 1.8GHz SOI Low-Noise Amplifier" *Electron Devices, IEEE Transactions on , Volume: 48 Issue: 4 , April 2001 Page(s): 803 –809.*

[5]B.Infguez,JP. Raskin, L.Demeus, A.Neve, D.Vanhoenacker, P.Simon, M.Goffioul, D.Flandre, "Deep-submicrometer DC-to-RF SOI MOSFET macro-model" *Electron Devices, IEEE Transactions on , Volume: 48 Issue: 9 , Sept. 2001 Page(s): 1981 –1988.*

[6] O, Kenneth, "Estimation methods for quality factors of inductors fabricated in silicon integrated circuit process technologies", *IEEE Journal of , Volume: 33 Issue: 8 , Aug. 1998 ,Page(s): 1249 –1252.*

[7] Philip Pieters, Kristof Vaesen, Steven bredels, Samir F. Mahmoud, Walter De Raedt, Eric Beyne, robert P.Mertens, "Accurate Modeling of High-Q spiral Inductors in Thin-film multilayer technology for wireless telecommunication applications". *IEEE transactions on microwave theory and techniques, vol49, No4, April 2001, p589-599.*

[8] S.Mahmoud, F.Beyne, "Theory and Techniques, Inductance and quality-factor evaluation of planar lumped inductors in a multilayer configuration", *IEEE Transactions on , Volume: 45 Issue: 6 , June 1997 Page(s): 918 –923.*

[9] IEEE Draft Supplement to IEEE Std 802.11, wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: High speed Physical Layer in the 5 GHz Band, September 1999.

[10] Workman, G.O. Fossum, "Physical noise modeling of SOI MOSFETs with analysis of the Lorentzian component in the low-frequency noise spectrum", *J. Electron Devices, IEEE Transactions on , Volume: 47 Issue: 6 , June 2000, Page(s): 1192 –1201.*